What is claimed is:

1. An integrated circuit comprising;

at least one quad state logic gate.

2. A logic gate comprising;

an input for receiving a signal, said signal encoding one of four logical states, circuitry for performing a logical operation on said received signal, and;

an output for transmitting a signal, said signal transmitted representative of said logical operation performed.

3. A method of performing Boolean logic operations using a single input, single output logic gate comprising;

inputting an encoded signal to said single input,

decoding two separate logic signals from said encoded signal,

performing a Boolean logic operation on said two logic signals, and;

outputting the result of said Boolean logic operation from said single output.

4. A circuit comprising;

a memory having an input and an output, said memory operable to store one of four voltage levels received at said input and to output said stored voltage level on said output,

a logic circuit having an input and an output, said logic circuit operable to perform a logical operation on voltage levels received at said input and to output the results of said logical operation on said output, and;

a connection formed between said memory output and said logic circuit input.

5. A logic gate comprising;

plural inputs for receiving signals, each of said signals encoding one of four logical states, circuitry for performing a logical operation on said signals received, and;

an output for transmitting a signal representative of said logical operation performed.

6. A circuit comprising;

a plurality of memories each having an input and an output, said memories operable to store any one of four voltage levels received at said input and to output said stored voltage level on said output,

a logic circuit having a plurality of inputs and an output, said logic circuit operable to perform a logical operation on voltage levels received at said inputs and to output the results of said logical operation on said output, and;

individual connections formed between each of said memory outputs to one of said logic circuit inputs.

7. A memory for storing any one of four voltage level inputs comprising; an input for receiving said voltage level inputs,

storage circuitry for latching said voltage level inputs,

circuitry for performing logical operations on said latched voltage levels, and;

an output for transmitting a signal indicative of the logical operation performed on said latched voltage levels.

8. A memory for storing an encoded signal comprising; an input for receiving said encoded signal,

storage circuitry for latching said encoded signal,

decode circuitry for extracting logic signals from said stored encoded signal, and;

a logic gate from performing a Boolean operation on said extracted logic signals.

9. A circuit comprising;

a quad state signal source for providing four state output signals,

a quad state memory for storing the signals output from said quad state signal source and outputting two state signal representations of logical operations performed on said quad state signals stored, and;

a two state signal destination for receiving the two state signals output from said quad state memory.

10. A memory for storing any one of four voltage level inputs comprising;

an input for receiving said voltage level inputs,

storage circuitry for latching said voltage level inputs,

circuitry for performing logical operations on said latched voltage levels,

a first output for transmitting said latched voltage levels from the memory, and;

a second output for transmitting a signal indicative of a logical operation performed on said latched voltage levels.

11. A circuit comprising;

a quad state signal source for providing four state output signals,

a quad state memory for storing the signals output from said quad state signal source,

said memory having first and second outputs,

said first output operable to output a signal representative of a logical operation performed on said stored quad state signal to a two state signal destination, and;

said second output operable to output the quad state signal stored to a quad state signal destination.

12. An integrated circuit comprising;

a quad state memory connected to a quad state logic gate.

13. An integrated circuit comprising; a quad state memory,

a quad state logic gate, and; a two state logic gate.

14. An integrated circuit comprising;

a quad state memory incorporating a quad state logic gate.

15. A process of reducing signal interconnects within an integrated circuit comprising; encoding two digital signals into one quad state signal, and

transmitting the quad state signal over a single interconnect.

16. An integrated circuit comprising;

quad state circuitry biased to operate between a first higher voltage and a lower voltage, and;

two state circuitry biased to operate between a second higher voltage and said lower voltage, said second higher voltage less higher than said first higher voltage.

17. A logic gate comprising;

a first input for receiving a signal, said signal encoding one of four logical states, a second input for receiving an output enable signals,

circuitry for performing a logical operation on said received signal,

an output for, when enabled by said second input, transmitting a signal representative of said logical operation performed.